

FIG. 1 (PRIOR ART)

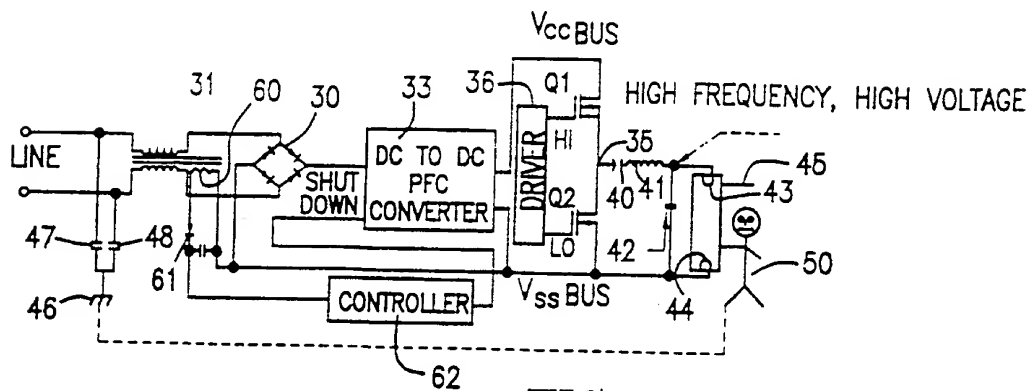


FIG. 2

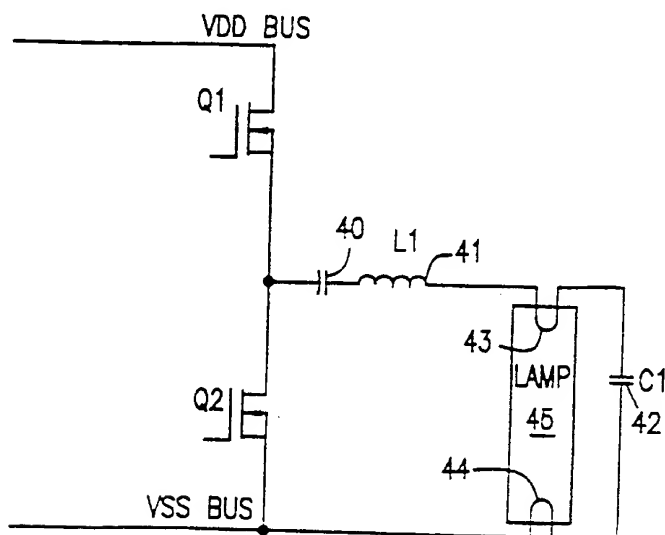


FIG. 3 (PRIOR ART)

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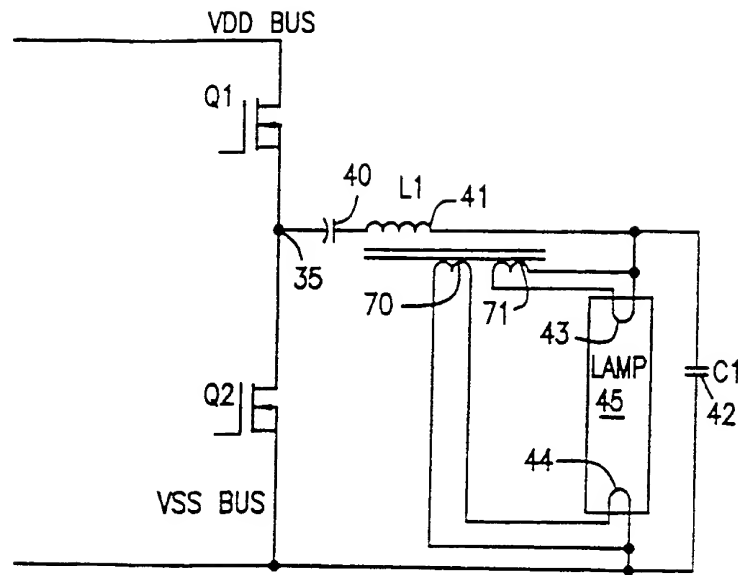


FIG. 4 (PRIOR ART)

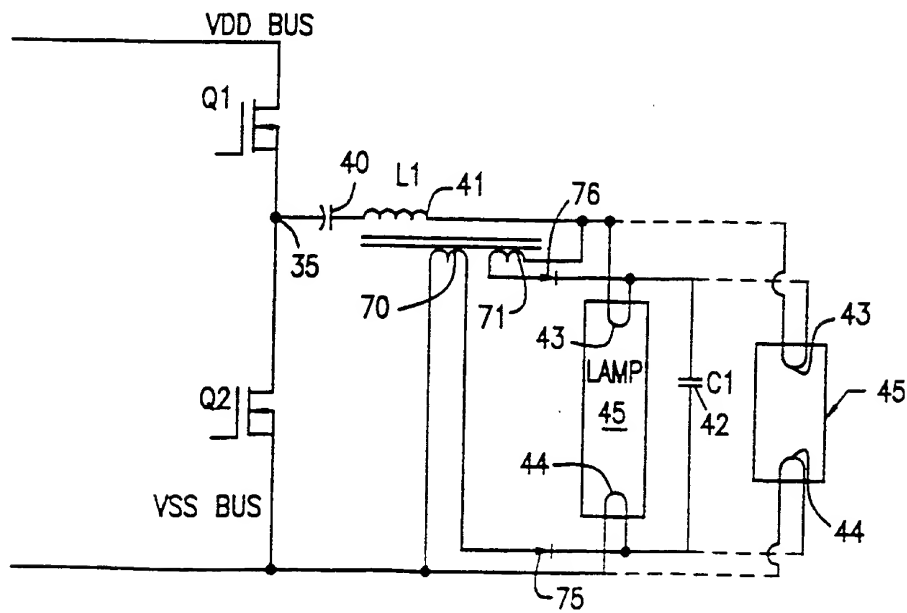


FIG. 5

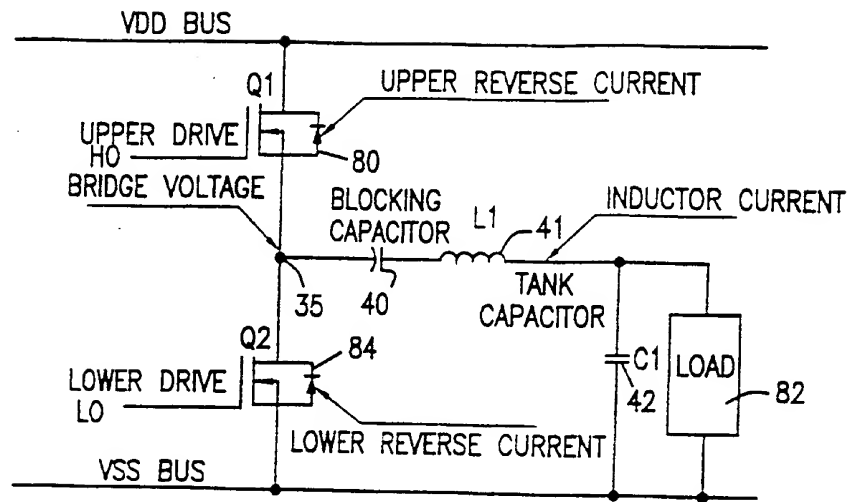


FIG. 6 (PRIOR ART)

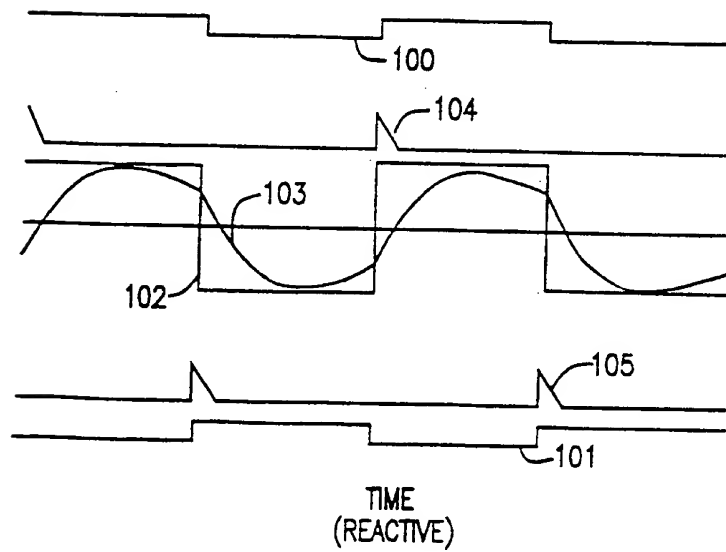


FIG. 7

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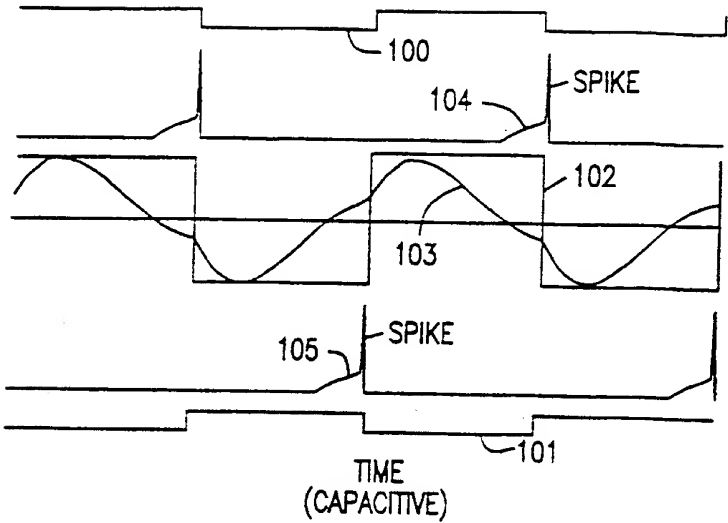
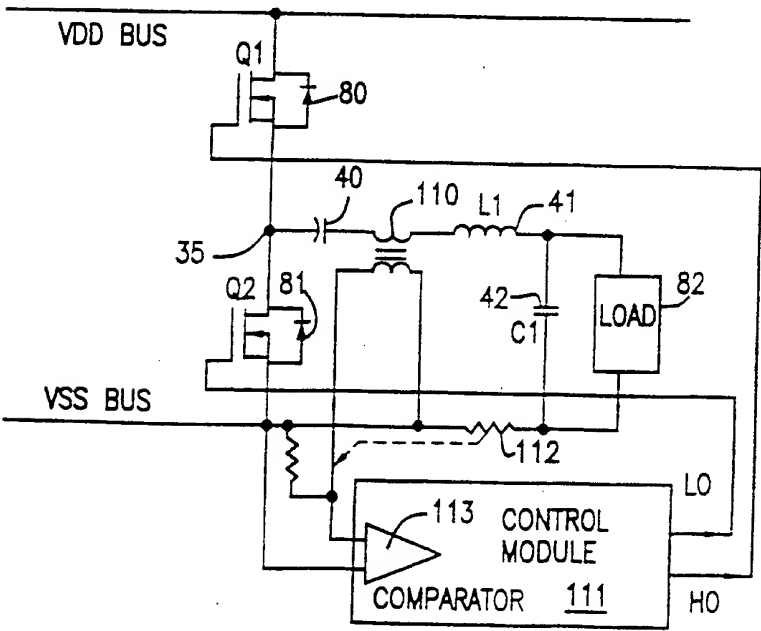
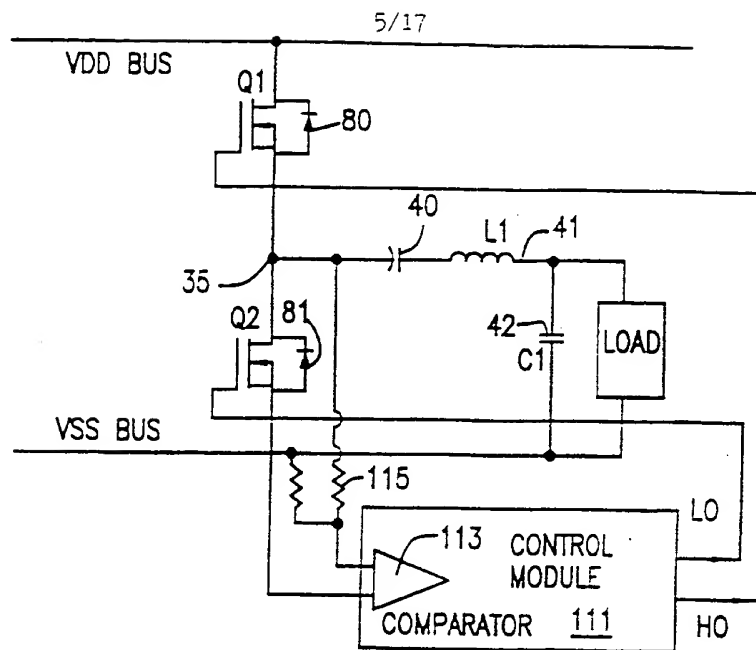


FIG. 8



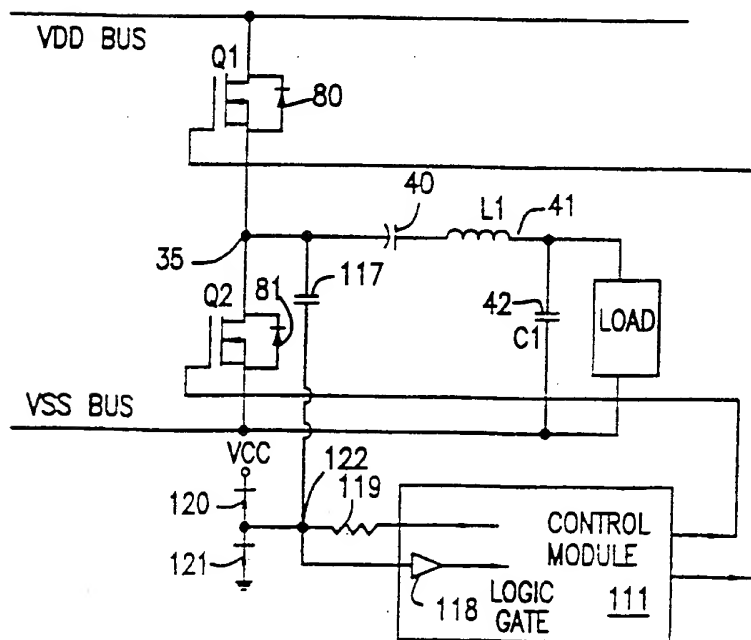
(CURRENT SENSE PROTECTION)

FIG. 9



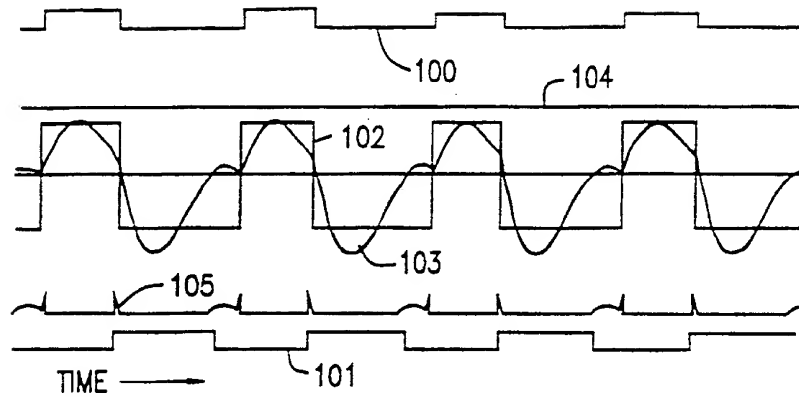
(VOLTAGE SENSE PROTECTION)

FIG. 10



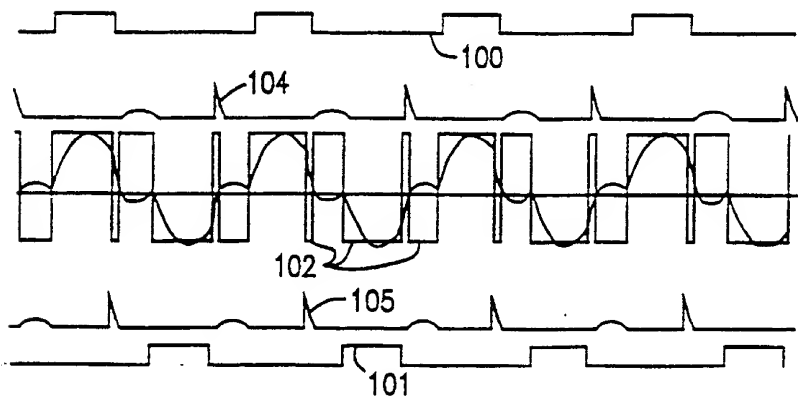
(DV/DT SENSE PROTECTION)

FIG. 11



(CONTINUOUS REACTIVE LOAD)

**FIG. 12**



(PREDICTED MINIMUM DEAD TIME)

**FIG. 13**

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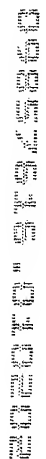


FIG. 14

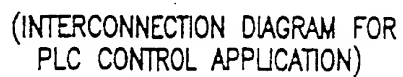


FIG. 15

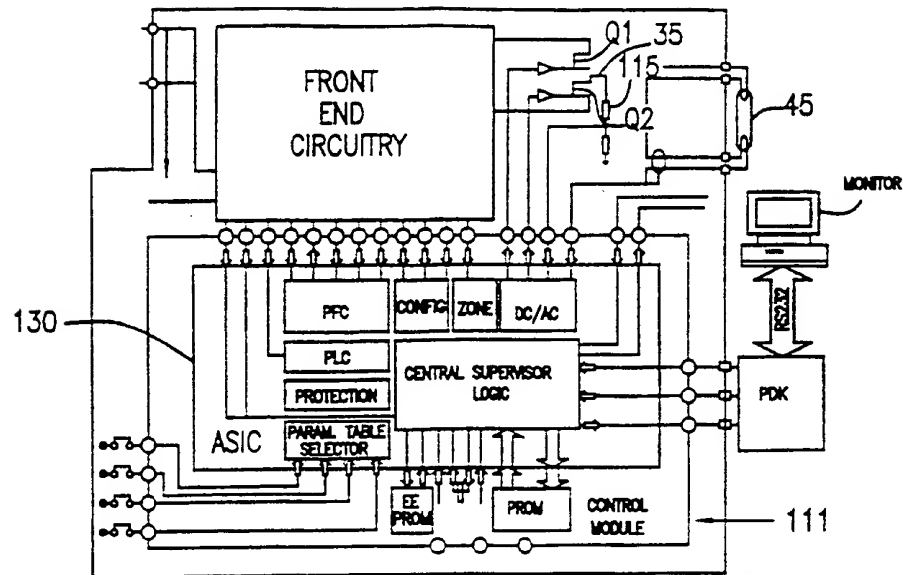
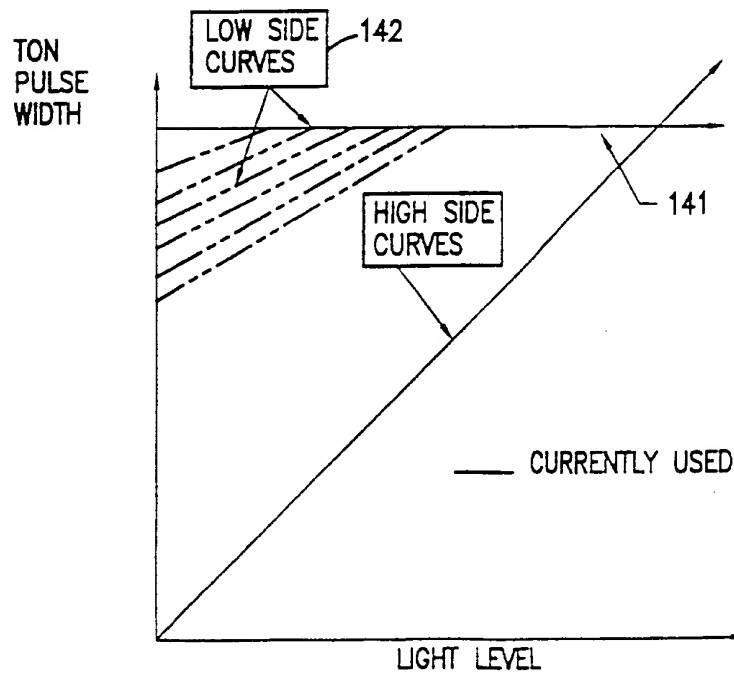


FIG. 16



(BRIDGE CONTROL GRAPHICAL DESCRIPTION OF RANGE OF THE PULSE WIDTH FOR THE BRIDGE SWITCHES)

FIG. 17



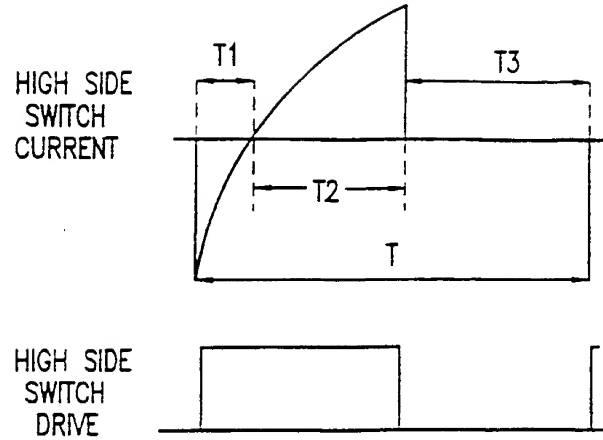


FIG. 17A

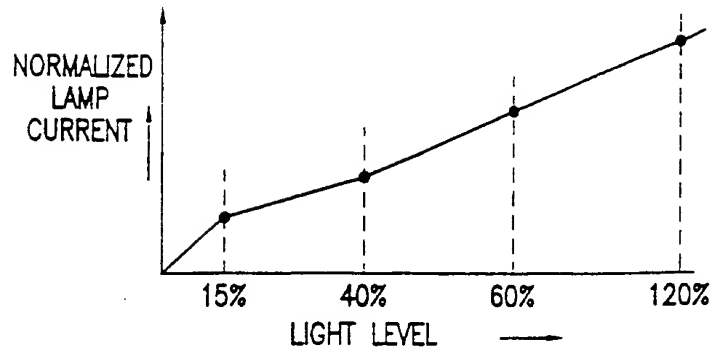
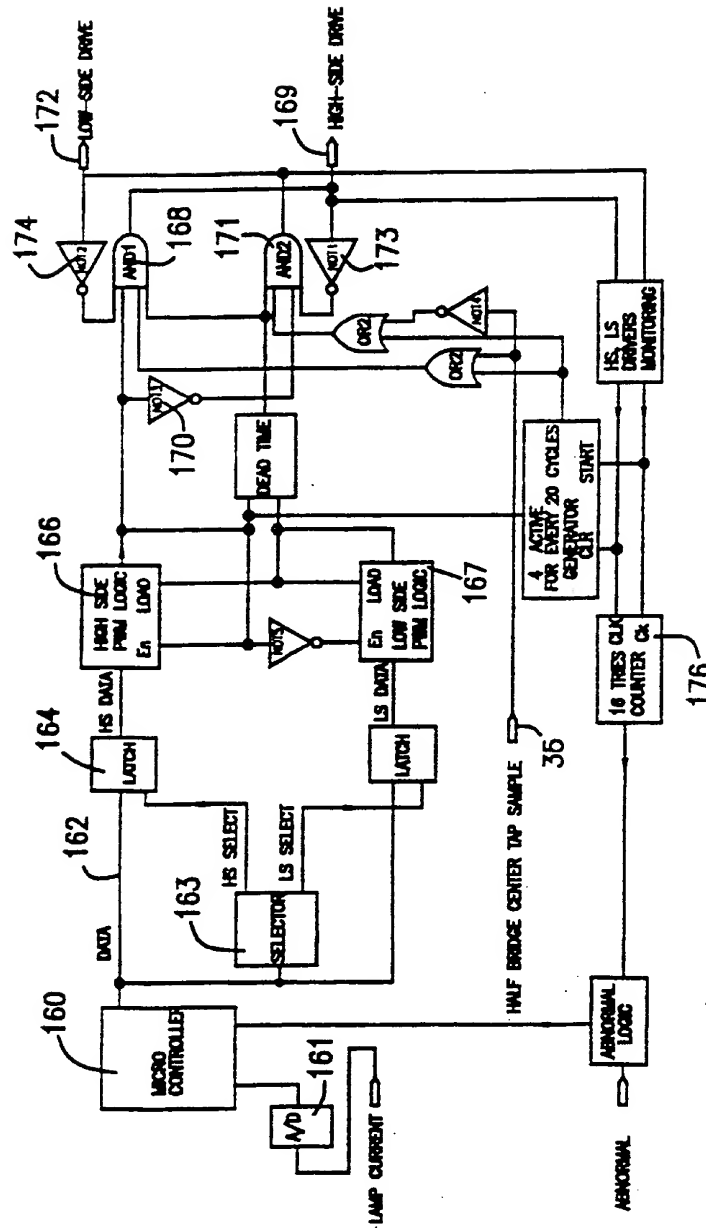


FIG. 20

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(ASIC DC/AC BLOCK DIAGRAM)

FIG. 18

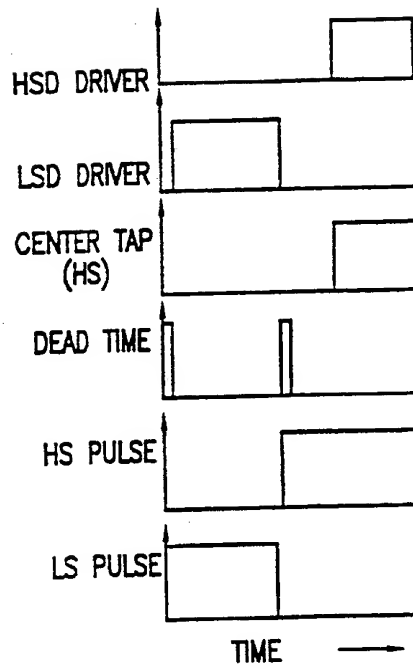


FIG. 19

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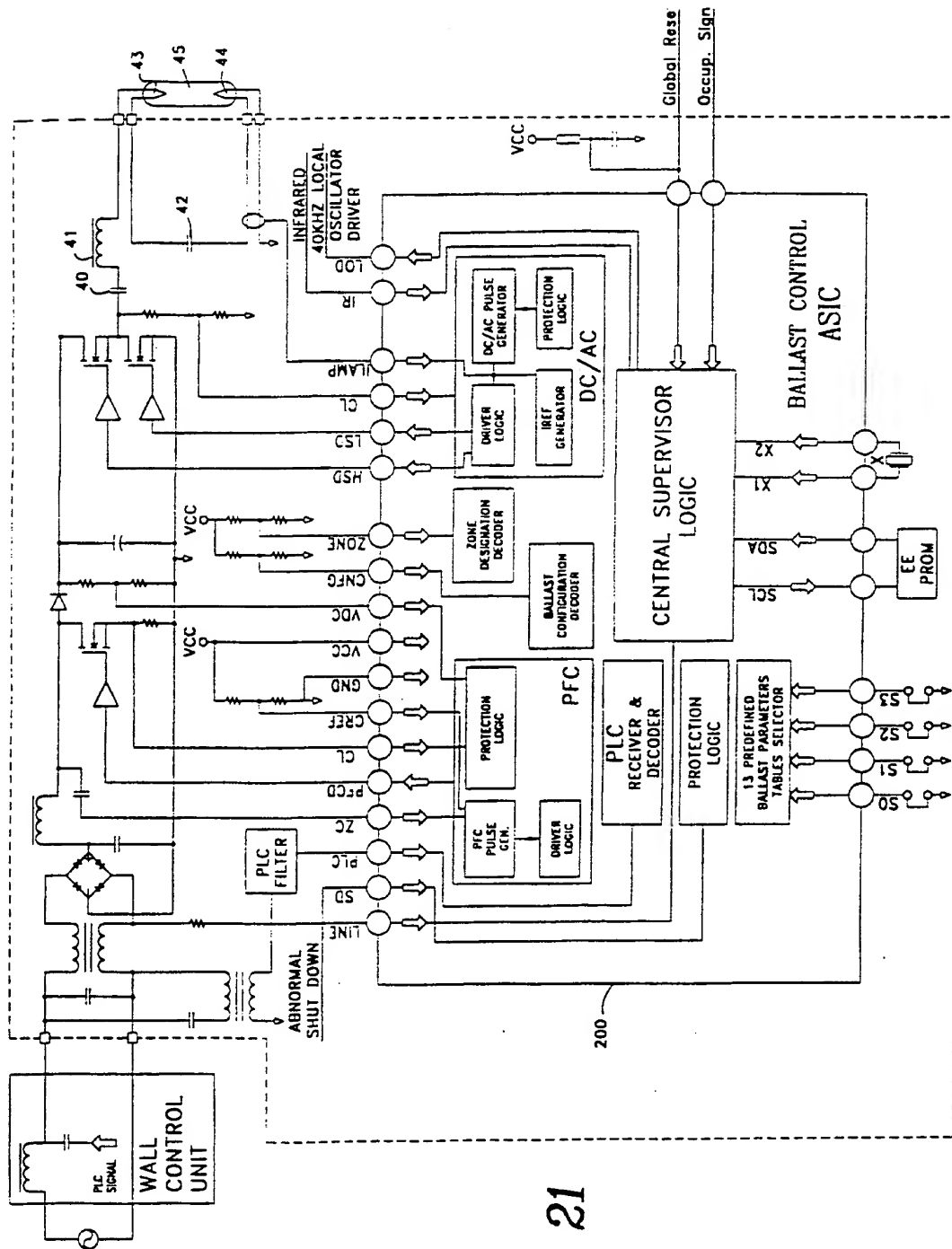


FIG. 21

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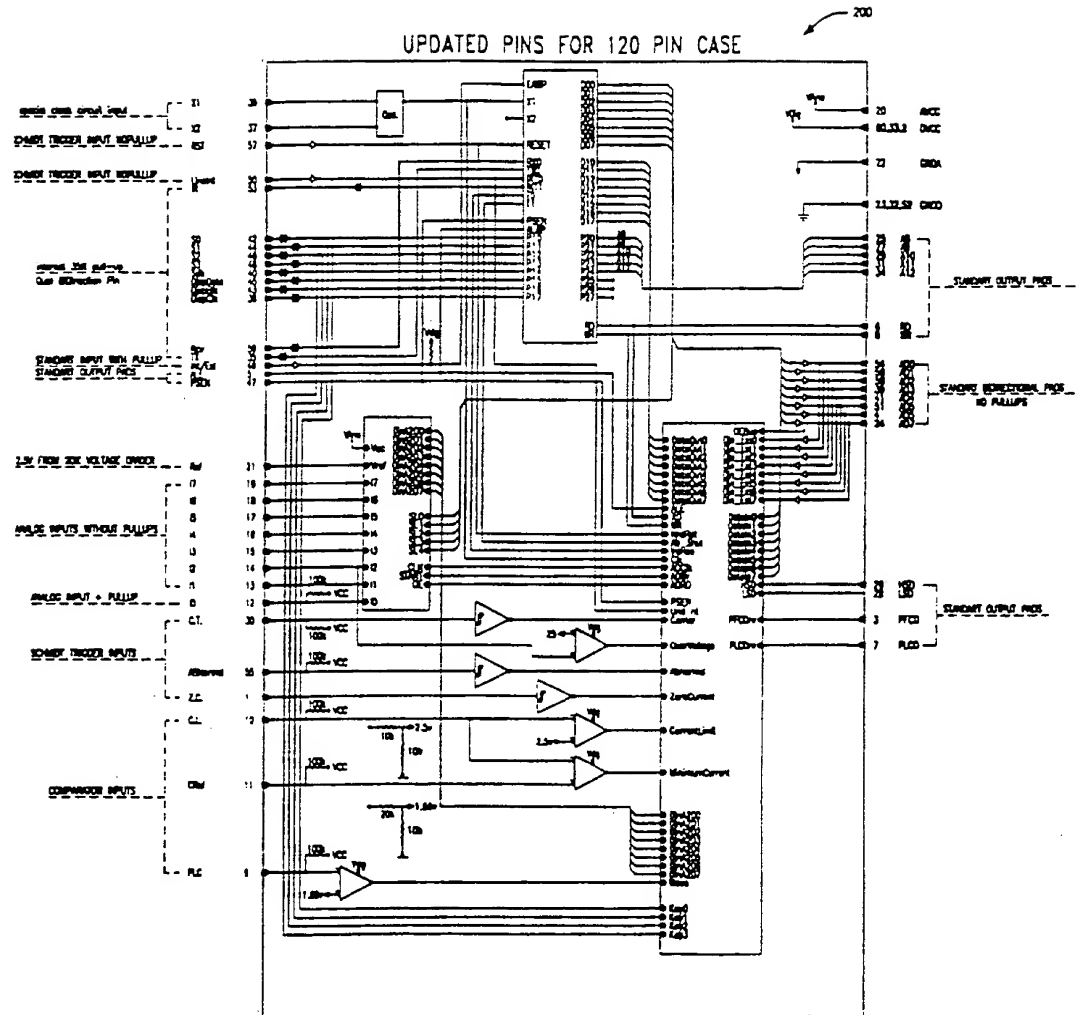


FIG. 21A

## ASIC PIN ASSIGNMENT

Die Pin Name	PLC D.E.B.	DC D.E.B.	LOCAL D.E.B.	OCC D.E.B.	E.B.	W.C.U.	Notes
Vcc Digital	+	+	+	+	+	+	
Gnd Digital	+	+	+	+	+	+	
X1-Crystal	+	+	+	+	+	+	
X2-Crystal	+	+	+	+	+	+	
Reset	+	+	+	+	+	+	
Vcc Analog	+	+	+	+	+	+	
Gnd Analog	+	+	+	+	+	+	
V Ref.	+	+	+	+	+	+	
10	30Kohm	0ohm	51Kohm	13Kohm	130Kohm	x	Analog
11	Zone	DC control	Sensor,Occ	Occ. Dimmed level	x	Sensor,Occ	Analog
12	VDC (dc bus)	VDC (dc bus)	VDC (dc bus)	VDC (dc bus)	VDC (dc bus)	x	Analog
13	ILamp	ILamp	ILamp	ILamp	ILamp	x	Analog
14,15,16,17	x	x	x	x	x	x	not used
Line Int.	+	+	+	+	+	+	
IR	x	x	+	x	x	+	
S0-S3	+	+	+	+	+	Key0-Key3	table
Scik	Scik	Scik	Scik	Scik	Scik	Scik	table
Tx	Sda	Sda	Sda	Sda	Sda	Sda	table
Rcv	x	x	Occ. OFF	Occ.	x	com. rcvr	
Disp. Blank	x	x	x	x	x	+	
Disp. Data	x	x	x	x	x	+	
Disp. Clk	x	x	x	x	x	+	
Abnormal	+	+	+	+	+	x	
Zero Curr.	+	+	+	+	+	x	
Curr. Ref.	+	+	+	+	+	x	
Curr. Limit	+	+	+	+	+	x	
Center tap	+	+	+	+	+	x	
PLC Drv	x	x	x	x	x	+	
H.S.D.	+	+	+	+	+	x	
L.S.D.	+	+	+	+	+	x	
PLC Data	+	x	x	x	x	x	
PFC Drv	+	+	+	+	+	x	
A00-A07	x	x	x	x	x	+	Ext ROM use
A8-A12	x	x	x	x	x	+	Ext ROM use
ALE	x	x	x	x	x	+	Ext ROM use
WR	x	x	x	x	x	+	Ext ROM use
RD	x	x	x	x	x	+	Ext ROM use
Int/ExtROM	x	x	x	x	x	+	Ext ROM use
Pean	x	x	x	x	x	+	Ext ROM use

FIG. 22

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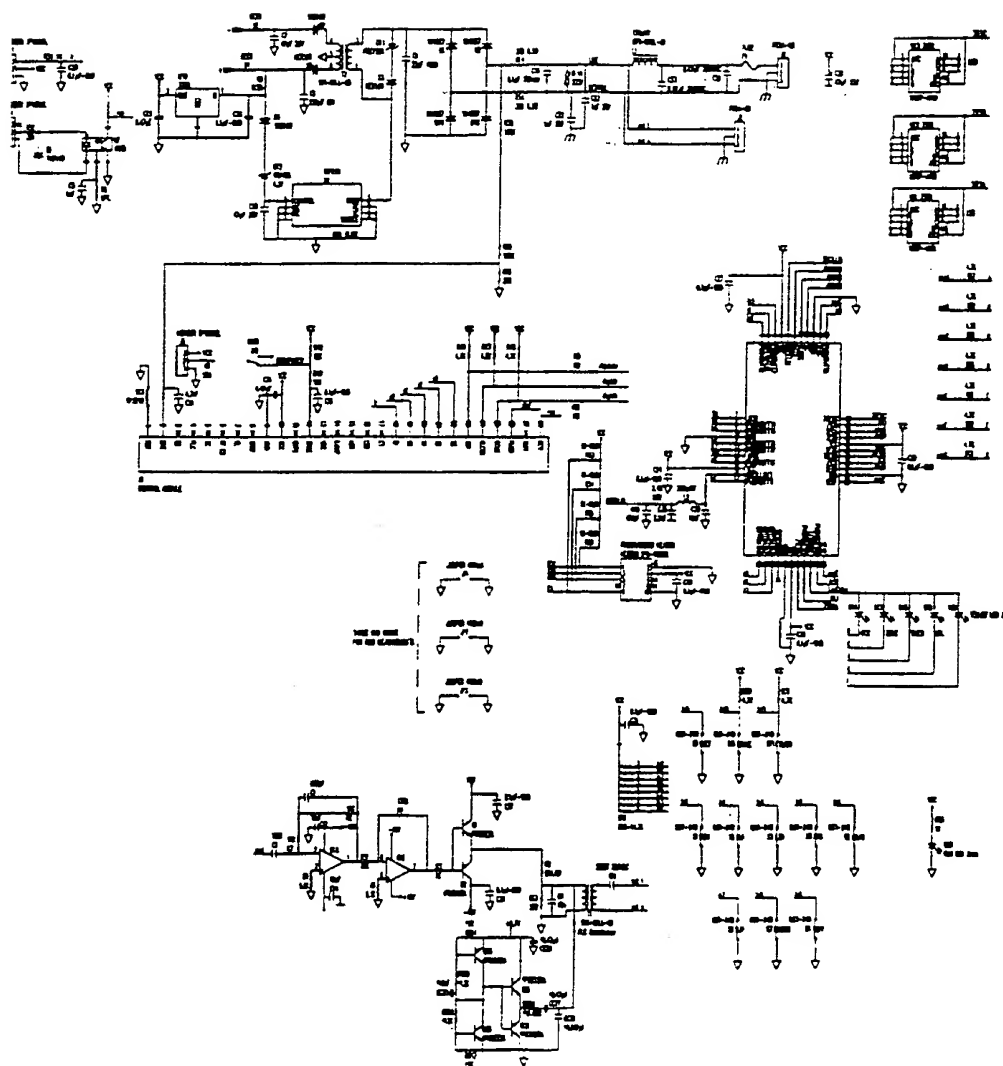


FIG. 23

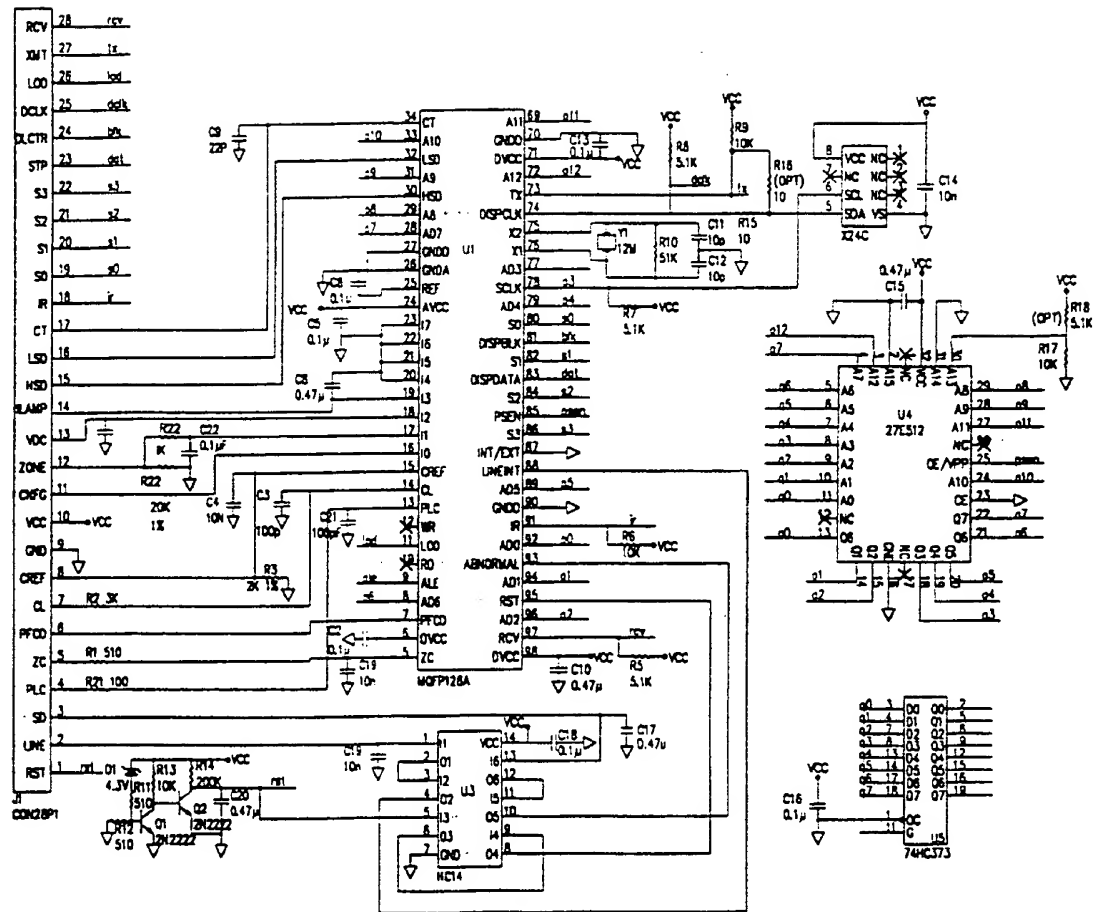


FIG. 24



FIG. 25

